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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,874	09/27/2000	Chou H. Li		7377

7590 03/28/2003

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EXAMINER
MANDALA, VICTOR A

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/670,874	LI, CHOU H.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *66-95* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *66,67,69-73,75-90,93 and 94* is/are rejected.

7)☐ Claim(s) *68,74,91,92 and 95* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *1-13-03* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Referring to the 35 U.S.C. 112 2nd paragraph rejections in the Office Action filed on, 9-1-02, the Applicant's Amendments, filed on 1-13-03, have overcome the previous rejections.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 87 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The examiner is unable to identify what the Applicant is claiming by **the thermal equilibrium phase-diagram values,** which is claimed in claim 87.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 66-67, 69-73, 75-82, 85-86, 88, and 93-94 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,057,584 Gardner et al.

3. Referring to claim 66, a solid state device comprising: a solid state material substrate, (Figure 2F #202), having a top surface; and a solid state material layer, (Figure 2F #204), no more than 10 Angstroms thick, (Col. 4 Lines 33-35), and positioned on the top surface of the substrate, (Figure 2F #202); at least a portion of the solid state material layer, (Figure 2F #204), being metallurgically bonded, (See ** below), to at least a selected portion of the top surface of the solid material state substrate, (Figure 2F #202).

** Initially, and with respect to claim 66, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

4. Referring to claim 67, a solid state device in which the solid state material layer has at least two of the following features: a) having an atomically smoothed bottom surface; b) having a curved top surface; c) having an atomically liquid-smoothed gate bottom layer; d) made of purified material; e) **made of strengthened material**; f) accurate to one atomic layer in thickness; g) aged by liquid diffusion; i) fine-grained or subgrained; j) oriented grains or subgrains; k) narrow grains or subgrains; and I) **stronger than unbonded material.**

5. Referring to claim 69, the device in which the solid-state material layer has an accuracy of better than several atoms on a layer dimension selected from the group consisting of thickness, depth, curvature, shape, size, chemical composition profiling, and lateral location, (Col. 4 Lines 33-35).

6. Referring to claim 70, a device in which at least a portion of the solid-state material layer, (Figure 2F #204), contains solid reinforcements, (Col. 4 Lines 15-18), whereby the bonded material layer is stronger than the unbonded solid state material, (Figure 2F #204), itself.

7. Referring to claim 71, a device in which the solid-state material layer, (Figure 2F #204), is sufficiently thin, (Col. 4 Lines 33-35), and flexible so as to yield under stress preventing device failure.

8. Referring to claim 72, a device in which the solid-state material layer is liquid diffusion aged, (See ** above).

9. Referring to claim 73, a device having a thickness of less than a micron thereby forming a thin-film integrated circuit device, it would be obvious to one having ordinary skill in the art at the time the invention was made to see that the device in Gardner et al.'s teachings would be less than 1 micron thickness when the gate oxide is between 5-10 Angstroms thick, (Col. 4 Lines 33-35), and the gate is 200 Angstroms thick, (Col. 6 Line 28).

10. Referring to claim 75, a device in which material of the solid state material layer, (Figure 2F #204), is purified by a melting and solidification process; the purity of material of the solid state material layer, (Figure 2F #204), being improved by at least one order of magnitude relative to the solid state material, (Figure 2F #204), prior to said metallurgically bonding, (See ** above).

11. Referring to claim 76, a device in which the solid-state material layer has an accuracy in thickness of one atomic layer, (See *** below).

*** Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the

Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

12. Referring to claim 77, a device in which the solid-state material layer comprises an ion implanted region, (Col. 4 Line 40), with a depth accurate to several atomic layers, (See *** above).

13. Referring to claim 78, a solid state device including: first and second solid state material pockets, (Figure 1 #103 & 105), positioned adjacent to each other, but laterally separated by a gap, on the top surface of the substrate, (Figure 2F #202); the solid state material layer, (figure 2F #204), filling and bridging the gap between the two adjacent solid state material pockets, (Figure 1 #103 & 105); and at least a portion of the solid state material layer, (Figure 2F #204), having an accuracy in thickness of better than three atomic layers, (See *** above).

14. Referring to claim 79, a solid state device in which: at least a part of the substrate, (Figure 1 #107), is a semiconductor of a first conductivity type; and at least one of the semiconductor pockets, (Figure 1 #103 & 105), is of a second conductivity type forming at least one PN junction region, (Col. 1 Lines 30-32), where the part of the substrate, (Figure 1 #107); contacts the at least one semiconductor material pocket, (Figure 1 #103).

15. Referring to claim 80, a device in which the solid-state material layer, (Figure 2F #204), is selected from the group consisting of a gate layer and a field layer.

16. Referring to claim 81, a device in which the substrate material is selected from the group consisting of Si, Ge, Si-Ge, InP, InSb, GaAs, SiC, InAs, superconductor, diamond, semiconductor material, intrinsic semiconductor material, substantially electrically insulating material, and substantially electrically conducting material, and mixture thereof, (Col. 1 Lines 18-20).

17. Referring to claim 82, a device selected from the group consisting of metal-oxide-semiconductor (MOS) device, (Col. 1 Lines 18-20), conductor-insulator-semiconductor (CIS) device, thin-film integrated circuit, and flexible integrated circuit.

18. Referring to claim 85, a device including a PN junction region, (Col. 1 Lines 30-32), having a curved, (Figure 1 #103 & 105), adjoining surface contacting the substrate, (Figure 1 #107), to thereby reduce but not eliminate at least one of inevitable thermal mismatch stress and in situ volume change strain generated during device processing, (See ** above); the remaining residual strain and stress on the curved adjoining surface of the PN junction region, (Col. 1 Lines 30-32), improving a selected device performance, (See */* below).

/ In reference to the claim language referring to [the function of the device improving a selected device performance], intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

19. Referring to claim 86, a device in which: the at least one PN junction region, (Col. 1 Lines 30-32), has a curved adjoining surface and; the at least one of the first and the second solid-state material pockets, (Figure 1 #103 & 105), meets the curved adjoining portion of the at least one PN junction region, (Col. 1 Lines 30-32).

20. Referring to claim 88, a device in which the solid state material layer, (Figure 2F #204), is an electrically insulating, wavy and curved field layer containing an ion-implanted [a] substance selected from the group consisting of oxygen and nitrogen, (Col. 4 Lines 15-18).

21. Referring to claim 93, a mass-produced solid state device comprising: a solid-state material substrate, (Figure 2F #202); at least one first solid state material pocket, (Figure 1 #103

& 105), positioned on a first selected surface of the substrate, (Figure 2F #202); and a solid state material layer, (Figure 2F #204), having at least one atomically smooth major surface which contacts and metallurgically bonds, (See ** below), the first selected surface of the substrate, (Figure 2F #202), to a first specified portion of the at least one first solid state material pocket, (Figure 1 #103).

** Initially, and with respect to claim 93, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

22. Referring to claim 94, a solid-state device further comprising: a second solid state material pocket, (Figure 1 #105), positioned on a second selected surface of the substrate, (Figure 2F #202), and laterally adjacent to, but separated by a gap from, the at least one first solid state material pocket, (Figure 1 #103); and in which: the solid state material layer, (Figure 2F #204), fills the gap between the two material pockets, (Figure 1 #103 & 105), while contacts and metallurgically bonds, (See **above), with a second specified portion of the second solid state material pocket, (Figure 1 #105).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 66, 78, 83-84, and 89-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2002/0164846.

23. Referring to claim 66, a solid state device comprising: a solid state material substrate, (Figure 4 #12), having a top surface; and a solid state material layer, (Figure 4 #14), no more than 10 Angstroms thick, (Paragraph 0021 Lines 1-7), and positioned on the top surface of the substrate, (Figure 4 #12); at least a portion of the solid state material layer, (Figure 4 #14), being metallurgically bonded, (See ** below), to at least a selected portion of the top surface of the solid material state substrate, (Figure 4 #12).

** Initially, and with respect to claim 66, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

24. Referring to claim 78, a solid state device including: first and second solid state material pockets, (Figure 4 #44a & 44b), positioned adjacent to each other, but laterally separated by a

gap, on the top surface of the substrate, (Figure 4 #12); the solid state material layer, (Figure 4 #14), filling and bridging the gap between the two adjacent solid state material pockets, (Figure 4 #44a & 44b); and at least a portion of the solid state material layer, (Figure 4 #14), having an accuracy in thickness of better than three atomic layers, (See *** below).

*** Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

25. Referring to claim 83, a device in which: the first and second solid state material pockets are respectively source and drain semiconductor pockets, (Figure 4 #44a & 44b), in a CMOS device and separated by a gap from each other; the solid state material layer, (Figure 4 #14), is a gate layer filling and bridging the gap between the two pockets, (Figure 4 #44a & 44b); and the gate layer material, (Figure 4 #14 and Paragraph 0021 Lines 1-7), has an atomically smooth surface at least on one of the top and major bottom surfaces thereof.

26. Referring to claim 84, a device in which each of a major portion of the substrate, solid state material pockets, and solid state material layer consists essentially of a single doped and less doped intrinsic semiconductor material, (Paragraph 0028 Lines 13-15), whereby the device is made resistant to dynamic forces due to impacts, vibrations, and large and rapid accelerations and decelerations, (See */* below).

/ In reference to the claim language referring to [the function of the device made resistant to dynamic forces due to impacts, vibrations, and large and rapid accelerations and decelerations], intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the

claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

27. Referring to claim 89, a device in which: the first and second solid state material pockets are respectively source and drain semiconductor pockets, (Figure 4 #44a & 44b), in a CMOS device; the solid state material layer is a gate layer, (Figure 4 #14); and including a conductive gate electrode, (Figure 4 #26a), of an electrically conducting material to control flow of electronic carriers from the source to the drain, (Figure 4 #44a & 44b).

28. Referring to claim 90, a device in which: the gate layer material, (Figure 4 #14), is atomically smoothed on at least one of top and bottom major surfaces thereof to achieve maximum smoothness; and material of the gate layer, (Figure 4 #14), being most purified at a bottom surface facing the substrate, (Figure 4 #12) and (See ** above).

Allowable Subject Matter

29. Claims 68, 74, 91-92 and 95 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Information Disclosure Statement

30. The information disclosure statement filed 1-13-03 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to

be listed. It has been placed in the application file, but the information referred to therein has not been considered. The Applicant did not submit Document No. 154,300, 816,626, 809,460, 313,350, 340,793, 08/483,937, 08/583,938, and 223-55.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
March 19, 2003

NATHAN J. FLYNN
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